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A Benchmark for Full Wave Electromagnetic Simulation of Optimized Planar Interconnects

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Abstract: **Full wave electromagnetic field solvers are essential tools in computer-aided microwave circuit design. When properly configured, commercial simulators are capable to analyze phenomena at microwave and millimeter-wave frequencies. Nonetheless, an assessment of the accuracy with which the simulation of ultra-broadband interconnects is accomplished becomes a difficult task. This is in part due to the large dependence of frequency-domain results with the selection of the computational domain of electromagnetic fields. This paper introduces a benchmark as a systematic method for the simulation of planar interconnects. Our method computes the line impedance to solve the size of numeric ports and the computational domain of fields. Its foundation lies on the modelling of microwave circuits allowing accurate predictions at high frequencies. The solution is validated by comparing simulation results with previously reported measurements of a Substrate Integrated Waveguide structure designed to operate in Ka band (26.5-40 GHz). It is seen that the method is well-suited for optimization of interconnects since the benchmark solution diminishes radiation losses associated to unwanted interactions with the bounding box. Our simulations make use of a commercial field solver based on finite difference time-domain method.**

Keywords: **Electromagnetic field solvers, Finite difference time domain, Planar interconnect, Line impedance computation and Substrate integrated waveguide.**

I. INTRODUCTION

Most microwave structures do not own exact analytical or semi-empirical equations of their characteristic impedance and propagation constant over a wide range of frequencies and therefore numerical solutions of EM (electromagnetic) fields play an important role in the analysis of high speed interconnects. EM solvers (full wave simulators [1-2] and 2.5D simulators [3-4]) have emerged as tools of widespread use that compute EM fields featuring different levels of accuracy. For instance, uniform planar interconnects with thick conductors can be analysed with good accuracy using 2.5D field solvers. On the other hand, planar interconnects for high-speed package systems are modelled more accurately by 3D solvers. Simulation results rely on computer models to analyse different phenomena that prevent planar interconnects from behaving as ideal transverse electromagnetic (TEM) structures. Losses, the dependence of substrate permittivity with frequency, inhomogeneous material systems; among other configurations, can be analysed by full wave simulation.

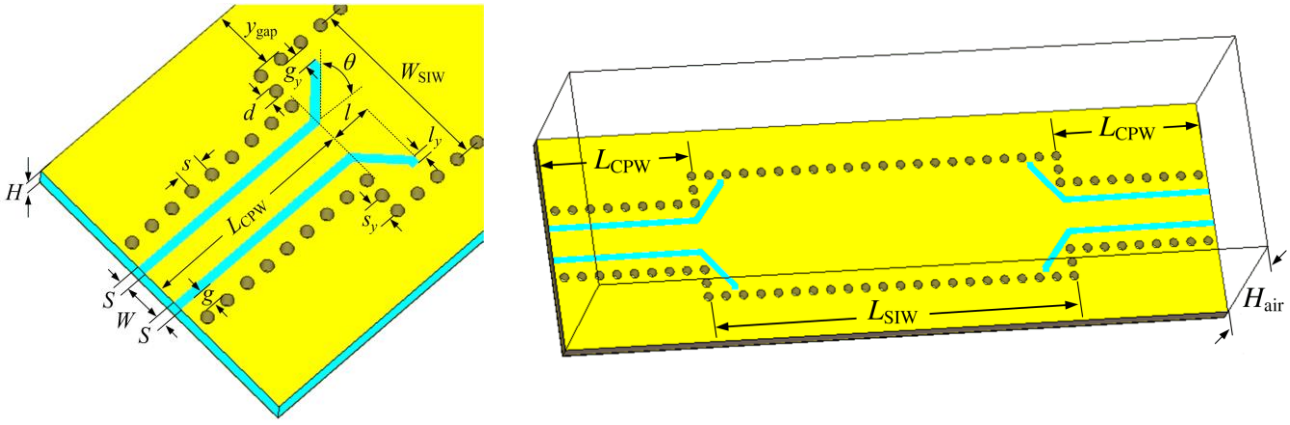
Nonetheless, when dealing with high-speed interconnects, there is not a general guideline to configure the 3D field solver. Frequency domain results depend greatly on the impedance mismatch between the port impedance (usually set to be equal to the TEM impedance, Z_0) and the impedance seen looking into the structure under analysis. Some deembedding procedures provided by commercial simulators can be applied to reduce port discontinuity. Nevertheless, field solutions of ultra-broadband interconnects are highly sensitive to parasitic couplings created with the boundary box. For instance, if the size of boundary box is not configured properly, scattering waves will undergo reflections with bounding surfaces which actually are configured to provide absorption conditions. Very often, the size of ports and bounding box are set to customary values however these parameters might be suitable only for narrowband designs. In this paper, we propose a benchmark as a systematic method to improve 3D EM simulations of ultrabroadband interconnects. The method is

illustrated with an interconnect based on a Substrate Integrated Waveguide (SIW). The method is developed employing Microwave Studio suit of CST™ [2].

II. SIMULATION OF INTERCONNECTS

The benchmark method is applied to the SIW structure shown in Fig. 1. This SIW with transitions to coplanar circuits was introduced in [5]. It comprises CBCPW-to-SIW transitions and conductor-backed coplanar waveguide (CBCPW) sections that feed power to Input/Ouput ports. CBCPW sections present simultaneously two modes of propagation, namely coplanar and microstrip modes. The microstrip mode is created by the lower ground plane which shields EM fields and allows large amount of power to propagate across the dielectric reducing dispersion and radiation losses. The dominant mode of propagation should be coplanar to make the waveguide nearly independent of the substrate thickness. The use of vias in CBCPW to ground upper planes facilitates the integration with a broadband SIW designed with via-fenced sidewalls. SIW section is constructed by conducting cylinders embedded in a dielectric substrate [6]. Table I itemizes the physical parameters of the SIW interconnection designed with Duroid® RT 6002.

Coplanar tapers and uniform SIW section are on an area of length, LSIW, equal to 21*s*. This length provides a sufficient extension for the EM fields to match the dominant mode of propagation within the SIW.



a) **b)**

Fig. 1. a) Detailed view of the transition CBCPW-to-SIW. b) SIW using transitions to CBCPW sections.

TABLE I: PARAMETERS OF THE SIW-BASED INTERCONNECT

Parameter	Value	Parameter	Value
H	0.508 mm	l_y	0.5 mm
W	0.9 mm	s_y	0.4085 mm
S	0.2262 mm	L_{CPW}	8.5*s*
d	0.3 mm	L_{SIW}	21*s*
s	2*d*	W_{SIW}	4.3 mm
g	0.358 mm		

Fig. 2 shows parameters of the benchmark. The boundary box consists of a top cover and lateral side walls defined as "open". The bottom cover is a conducting wall with conductivity equal to 5.88×10^7 S/m (copper), which is the same conductivity as that used in ground plane. The use of Numeric Ports requires Perfect Electric Conductor as boundary conditions. The bounding box parameters are the distance between the upper ground plane to the port edge, h, the distance between the port to the top cover, H_{top}, the port width, W_{port}, and the distance between the outer edge of the external rows of vias to the lateral walls, y_{gap}.

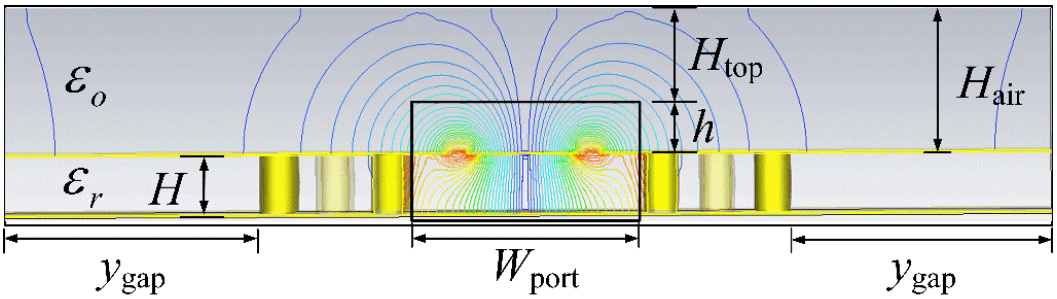


Fig. 2. 2D-perspective of configuration of the benchmark solution

The solution of the complete structure must be associated to a monomode interconnect. For instance, W_{port} is set to cover most of the EM fields around both line slots so as to improve power coupled to the waveguide. For a CBCPW with upper planes grounded by conductive walls, CST handbook [7] suggests choosing a W_{port} in the interval ($2w$, $3w$), given by $w = W + 2S$. However, it was found that higher order modes of propagation arise if the ports cover any part of the row of vias section. Monomode operation is ensured if W_{port} is lower than $W + 2S + 2g - d$, then W_{port} must be lower or equal to $1.307w$, which is smaller than the minimal port width recommended, $2w$. A set of geometrical constrains must be defined through simulations not only to ensure monomode operation but also to reduce field leakage.

The impedance seen looking into the Port 1 of the interconnect terminated with the port impedance is given by [8]:

$$Z_{in} = \frac{P_s - P_{loss} + 2j\omega(W_m - W_e)}{II^*/2} \quad (1)$$

where P_s is the average-power provided by the source, P_{loss} is the average power losses that correspond to reflections at the far-end port, ohmic, dielectric and radiation losses. I is the average current at the input port and ω is the angular frequency. W_m and W_e correspond to the average magnetic and electric energy, respectively, in the volume enclosed by the bounding box. The reactive component of the impedance in Eq. 1 depends directly on the difference between the stored magnetic and electric energies in the structure. Low-loss planar waveguides exhibit higher Quality (Q-) factors and very low reactive impedance. In the following, Z_{in} is shown to present only a resistive characteristic in the frequency band of interest.

The line impedance in Eq. 1 computes the effective power transported by the quasi-TEM wave in the direction of propagation. To obtain accurate results, the benchmark method computes the line impedance using the definition of characteristic impedance. For coplanar waveguides, the power-to-current definition provides a more accurate calculation of the characteristic impedance [9].The current in Eq. 1 is evaluated via the line integral of the magnetic field. At higher frequencies, the quasi-TEM behaviour of the waveguide produces a displacement current that flows over the surface formed by the contour of the curve. In order to reduce the dependence of the calculation on the shape of the curve used, we implement a curve that encloses tightly the cross section of the central conductor thereby the line integral computation yields a good approximation to the actual current flowing on the signal trace. The Microwave suite of CST can compute the line impedance as a post-processing step.

III. OPTIMIZATION GOAL

In the proposed method, the interconnect under analysis is considered as a two-port microwave circuit shown in Fig. 3. The TEM characteristic impedance of the transmission line structure, Z_0, is equal to the reference impedance used to normalize the S-parameters. In the back-to-back configuration of the structure, Zs and Z_l, are set to be equal to Z_0 in correspondence to the impedance of the input and output ports; respectively. Mismatch between the impedance of the numeric port and the input impedance of the interconnect leads to reflection and insertion losses. The input reflection coefficient normalized to the TEM characteristic impedance of the interconnect is given by:

$$\Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \quad (2)$$

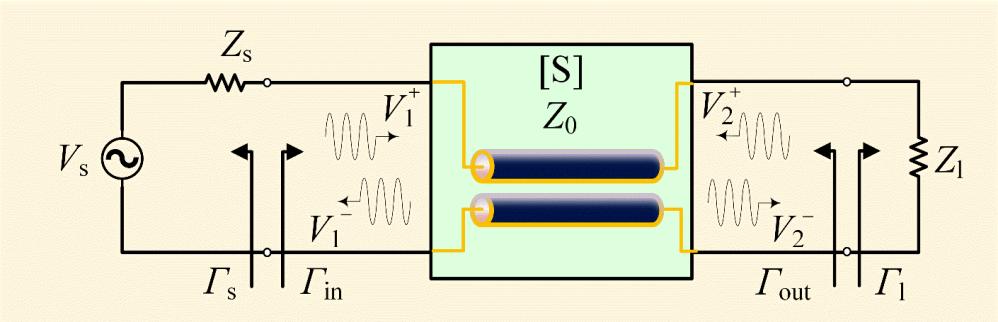


Fig. 3. Microwave circuit model of the interconnect

The input scattering reflection parameter, S_{11}, can be calculated using the ratio between the reflected and incident voltage waves at the input port. However, at high frequencies, reflections at the far-end port arises and therefore the input reflection coefficient, Γ_{in}, results to be different from S_{11}. The analysis of the structure using the two-port circuit representation in Fig. 3 yields to:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_l}{1 - S_{22}\Gamma_l} \qquad (3)$$

Where Γ_l is the reflection coefficient at the load.

The analysis based on Eq. 3 requires computing all the S-parameters of the waveguide and turns out to be more complicated for use in the proposed method. For lossy waveguides, the analysis based solely on $|S_{11}|$ does not allow determining if there is room for improving performance as this parameter varies greatly with frequency. Rather, the line impedance computation is a foundation for our proposal. The input coefficient reflection given by (2) allows establishing the optimization goal straightforwardly. The benchmark method computes the line impedance at the maximal frequency of interest, ω_{max}, and the solution requires solving the optimization problem:

$$\boldsymbol{U}^* = \arg \min_{\boldsymbol{U} \in \boldsymbol{B}} \left(Z_0 - Z_{in}(\omega_{max}) \right) \qquad (4)$$

where elements of the vector $\boldsymbol{U}$ correspond to geometrical variables of the bounding box and numeric port. Those parameters are swept within a design space $\boldsymbol{B}$, which is determined by geometrical constrains of the interconnect that ensure monomode operation. For the SIW-based interconnect, the benchmark variables are $\boldsymbol{U} = [y_{gap}, H_{top}, h, W_{port}]^T$.

Convergence of the benchmark solution is achieved by relying on a low number of meshcells per wavelength, as used to compute the EM fields surrounding the interconnect with suitable accuracy. This leads to achieve a sweep analysis that consumes low computational time without requiring fine mesh resolutions to perform accurate analysis of the interconnect.

IV. BENCHMARK SOLUTION

The performance of the SIW-based interconnect depends on the tapers that convert coplanar mode to the dominant transverse electric mode of the SIW, TE_{10}. The conversion of monomode wave impedances in the structure requires tuning the aperture angle, θ, and the length of the linear taper, l (see Fig. 1.a). Experimental work by Chen and Wu [5] makes use of a numerical calibration technique termed Thru-Reflection-Line (TRL) for optimizing impedance transformation of the tapers. An optimal impedance transformation is achieved at the vector $\boldsymbol{x} = [\theta\ l]^T = [45\ 1.05]^T$. Those parameters allows validating the technique in a fabricated prototype. The complete structure with CBCPW-to-SIW converters was simulated and optimized in [10]. Surrogate modeling becomes appealing for optimization of the SIW-based interconnect since it does not involve time-consuming direct optimization. The model was constructed using an initial vector $\boldsymbol{x}^{(0)} = [45\ 1]^T$ and the evaluation of surrogate polynomial interpolants led to optimize $|S_{11}|$ of the complete interconnect. By simulating at different design points and mesh resolutions, the optimal model results in the vector $\boldsymbol{x}^* = [49.73\ 1.03]^T$. However, the optimization goal of the fabricated prototype ($|S_{11}| < -20$ dB) was not fully accomplished over the entire Ka-band by the surrogate optimization. In the following, we demonstrate that the use of the bounding box parameters set to predetermined parameters, $H_{air} = 10H$ and $y_{gap} = 1.66$ mm, as reported in [12] results in little room for optimization.

The benchmark solution makes use of one-by-one sweep analysis of the set of variables (y_{gap}, H_{top}, h, W_{port}) in a design space where the interconnect works as a monomode waveguide. In the following, the benchmark solution employs design parameters for optimal impedance transformation referred above, $\boldsymbol{x} = [\theta, l]^T = [45\ 1.05]^T$. We have no information on the stub length. To avoid significant field leakage in the taper, we choose g_y to be equal to 0.05 mm, yielding $l_y = 0.5$ mm.

Table II shows the computation of the input impedance at 40 GHz. In Sweep 1 column, the input impedance reaches its maximum when $y_{gap} \geq 3.70w$ then we choose $y_{gap} = 3.70w$. In this sweep, W_{port} is fixed to w, so that port lateral edges are sufficiently separated from the rows of vias creating low field scattering. h was set to be equal to $w/2$, as recommended by CST handbook for coplanar waveguides [7]. H_{top} was set to be equal to H. Other analysis involves the variation of the distance, H_{top}. The sweep function is given on the Second column of Table II in which Z_{in} has its maximum at $H_{top} = H/2$. In another sweep analysis, we vary the port height h, finding more sensibility of the input impedance to this parameter when compared with previous analyses. As show on the Sweep 3 column, the best value is obtained when $h = 1.55w$.

Finally, a sweep analysis of the port width is performed and results are shown on Sweep 4 column. The best value corresponds to the maximum port width, $W_{port} = 1.307w$. However, the proximity of the rows of vias with the port has an important effect to be taken into consideration. When the port lateral edges are close to the rows of vias, coplanar line sections presents significant field leakage. CBCPW were analyzed in other set of simulations without tapers and SIW sections. We notice that when W_{port} is large (higher than $1.25w$), $|S_{11}|$ presents larger reflections at very low frequencies and its frequency nulls present misalignment spoiling the overall performance. We choose w as the port width that introduces the minimal field leakage.

The benchmark solution for the variables (y_{gap}, H_{top}, h, W_{port}) is the vector $\boldsymbol{U^*} = [3.7w, 0.5H, 1.55H, w]^T$. CST simulations were run on a computing platform based on desktop with Pentium R processor at 3 GHz and 8 GB RAM. Each Sweep consumes approximately the same computation time, 28 min and the number of mesh cells is about 750k. Both, the starting lines per wavelength and the lower mesh limit are set to be equal to 15. For the port impedance computation, 4 passes with a refinement factor equal to 0.7 were required.

TABLE II: INPUT IMPEDANCES COMPUTED BY THE POWER-TO-CURRENT RATIO

SWEEP 1		**SWEEP 2**		**SWEEP 3**		**SWEEP 4**	
y_{gap}/w	Z_{in} (Ω)	H_{top}/H	Z_{in}(Ω)	h/H	Z_{in}(Ω)	W_{port}/W	Z_{in}(Ω)
1.00	41.55	0.10	41.72	0.50	42.27	**1.00**	46.35
2.35	41.68	0.25	42.81	0.85	45.12	1.07	46.69
3.70	42.74	**0.50**	42.89	1.20	46.16	1.13	47.77
5.05	42.74	0.75	42.79	**1.55**	46.35	1.25	48.81
10.0	42.74	1.00	42.75	1.90	46.19	1.38	49.06
		1.25	41.93	2.25	45.61	1.44	49.35
		1.50	41.89	2.5	43.93	1.52	49.93

Figure 4 displays measured and simulation results of the interconnect. The difference between parameters results to be lower than 3 dB over the half part of the Ka band (33-40 GHz, excepting near the frequency null). Since the transition of the waveguide was fabricated as an optimized impedance transformer and our EM modeling provides good performance predictions at high frequencies, the benchmark solution allows optimized responses, as confirmed shortly.

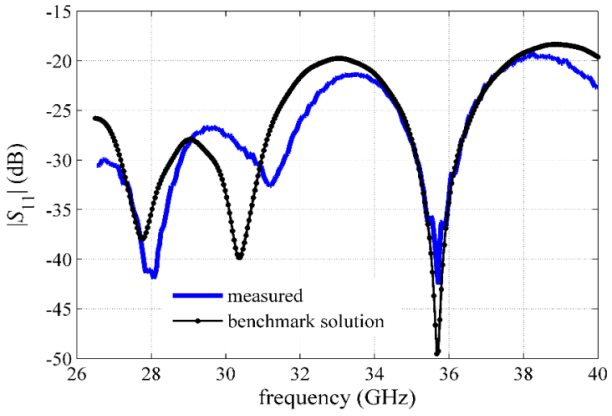
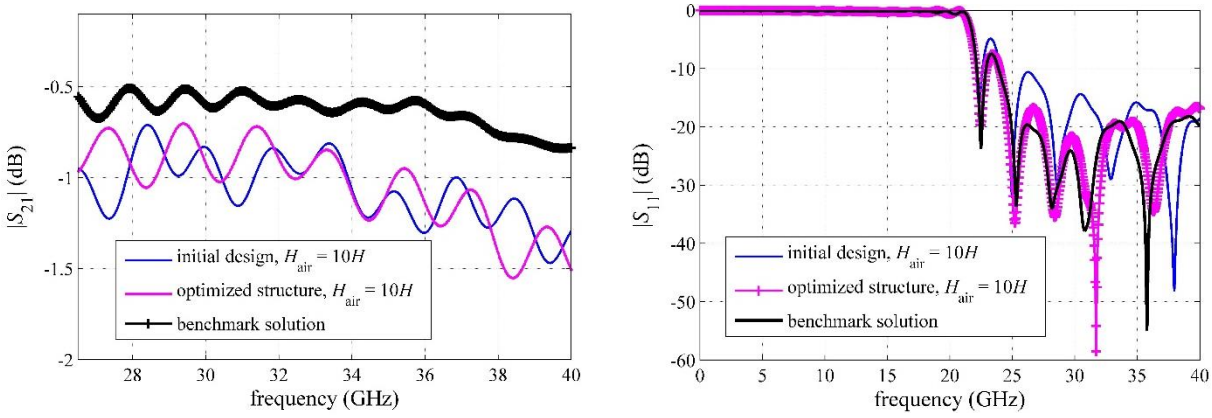


Fig. 4. Measurements (taken from [5]) and simulation results of the SIW-based interconnect.

Fig 5 allows contrasting responses of the interconnect using parameters reported in [10] and those obtained by the benchmark. The insertion loss of the design based on the benchmark solution is about 0.4 dB lower with respect to structures simulated with a boundary box dimensioned with customary parameters. The predicted insertion loss is about 0.6 dB, which is closer to the 0.4 dB reported for the fabricated transition.



a) **b)**

Fig. 5. Frequency parameters of SIW-based interconnect using the parameters reported in [10] and results of the benchmark. a) $|S_{21}|$ and b) $|S_{11}|$.

The benchmark solution results in a structure with lower scattering reflection parameters at high and low frequencies. Notice that implementations using the initial, $x^{(0)}$, and optimized, x^*, design vectors do not show clear performance improvements over the Ka-band.

The analysis of radiation losses in the bounding box allows an assessment of the solution. This can be computed by an EM modeling based on loss-free Rogers RT6002 dielectric and Perfect Electric Conductor in metals. The power loss is computed by $|S_{11}|^2 \square\square |S_{21}|^2$ [6] and the resulting losses are associated only to radiation. Figure 6 displays results of the structures.

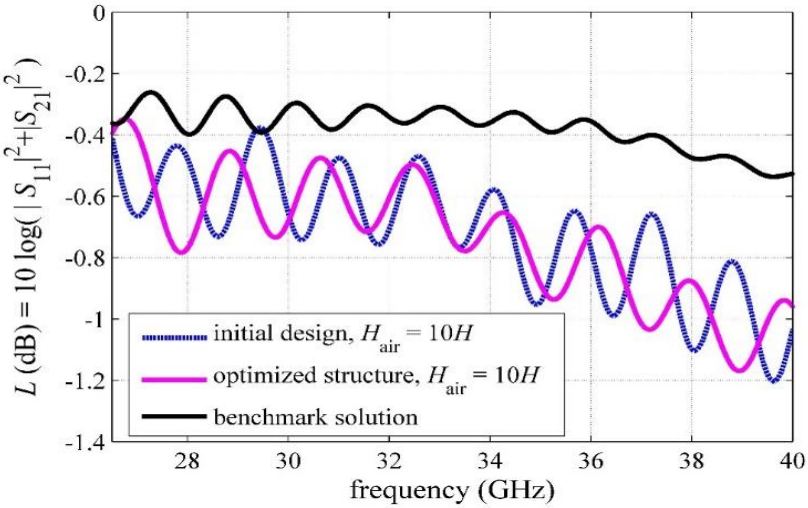


Fig. 6. Radiation losses of the SIW-based interconnect in the Ka-band.

It is apparent that a large distance from the upper metal of the interconnect to the top cover of the bounding box (equal to 10*H*) creates larger radiation losses regardless the optimized taper variables. At 40 GHz, the benchmark solution improves radiation losses about 0.5 dB over the level obtained by designs based on customary box parameters.

Those results indicate that a minimization of the parameter $|S_{11}|$ on its own is not a sufficient condition to optimize overall performance. Additionally, the optimization must consider effective solutions to diminish radiation losses.

V. CONCLUSION

This paper introduces a methodology based on the line impedance computation as a post-processing step of EM analysis to find a better way to configure boundary box and numeric ports. Our method was applied to a SIW structure with transitions optimized to coplanar circuits. Despite the lack of information on some variables of the SIW-based prototype reported in the open literature, the EM modeling based on the benchmark solution presents low discrepancies; lower than 3 dB over the half part of the Ka-band. Our results indicate that solving the electromagnetic domain not only allows achieving accurate predictions of practical interconnects at higher frequencies but also reduces radiation losses over the whole frequency band. Therefore, the benchmark solution could be considered as an initial design of an accurate 3D model involving low computational cost. In this work, the benchmark method was developed using a simulator based on the finite difference time-domain method, however it could be applied to other commercial field solvers featuring similar field computing capabilities.

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